SN 10/620, 179

Docket Number (Optional) Application Number Form PTO-1449 3351.8US (96-0223.07/US) Not yet assigned INFORMATION DISCLOSURE CITATION Applicant Brent Ke th IN AN APPLICATION (Use several sheets if necessary) Filing Date July 14, 2003 Group Art Unit Uniknown **U.S. PATENT DOCUMENTS EXAMINER** FILING DATE DOCUMENT NUMBER DATE NAME CLASS SUBCLASS INITIAL IF APPROPRIATE W 4,536,947 08/1985 Bohr et al. 4,742,018 05/1988 Kimura et al. 4,914,502 04/1990 Lebowitz et al. 4,922,460 05/1990 Furutani et al. 4,967,396 10/1990 Kajigaya et al. 4.970.564 11/1990 Kimura et al. 5,014,110 05/1991 Satoh 5,107,459 04/1992 Chu et al. 5,138,412 08/1992 Hieda et al. 5,170,243 12/1992 Dhong et al. Via O. Nauyen Primary Examiner M 04/1993 5,206,183 Dennison 5,208,180 05/1993 Gonzalez 5,243,558 09/1993 Saeki FOREIGN PATENT DOCUMENTS Translation DOCUMENT NUMBER DATE COUNTRY CLASS SUBCLASS NO YES 3-174765 07/1991 Japan 60-258795 12/1984 Japan 4433695 03/1995 Germany 0078338 05/1983 **EPO** OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.) Ahn et al., "Bidirectional Matched Global Bit Line Scheme for High Density DRAMS", (Abstract), pps. 91-92. Hamada et al., "A Split -Level Diagonal Bit-Line (SLDB) Stacked Capacitor Cell for 256MbDRAMs", IEEE, April; 1992, pps. 799-802. Inoue et al., "A 16Mb DRAM with An Open Bit-Line Architecture", International Solid State Circuits Conference, IEEE, 1988, pps. 246-247. **EXAMINER** DATE CONSIDERED V. Naugen EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conforman

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Sheet 2 of 4

Form PTO-1449 Docket Number (Optional) Application Number 3351.8US (96-0223.07/US) Not yet assigned INFORMATION DISCLOSURE CITATION **Applicant Brent Keeth** IN AN APPLICATION (Use several sheets if necessary) Filing Date July 14, 2003 Group Art Unit Unknown **U.S. PATENT DOCUMENTS** EXAMINER FILING DATE DOCUMENT NUMBER DATE CLASS SUBCLASS INITIAL IF APPROPRIATE 5,280,443 01/1994 Hidaka et al. 5,315,542 05/1994 Melzner 5.396.450 03/1995 Takashima et al. 5,396,451 03/1995 Ema 5,499,205 03/1996 Ahn et al. 5,534,732 07/1996 DeBrosse et al. 5,581,126 12/1996 Moench 5,625,234 04/1997 Suzuki et al. 5,670,815 09/1997 Childs et al. 5,680,347 10/1997 Takeuchi et al. VIX Q. Ngujen 5,815,428 09/1998 Tsuruda et al. 5,838,038 11/1998 Takashima et al. 5,864,181 01/1999 Keeth 5,877,976 03/1999 Lattimore et al. FOREIGN PATENT DOCUMENTS Translation DOCUMENT NUMBER DATE COUNTRY CLASS SUBCLASS YES NO **OTHER DOCUMENTS** (Including Author, Title, Date, Pertinent Pages, Etc.) Kimura et al., "A Block-Oriented RAM with Half-Sized DRAM Cell and Quasi-Folded Data-Line Architecture", November 11, 1991, IEEE, Journal of Solid-State Circuit, pps. 1511-1518. Takashima et al., "Open/Folded Bit-Line Arrangement for Ultra High-Density DRAMs", (Abstract), pps. 89-90. Hidaka et al., "A Divided/Shared Bit-Line Sensing Scheme for ULSI DRAM Cores", Journal of Solid-State Circuit, Vol. 26, No. 4, April 1991, pps. 473-477. **EXAMINER** DATE CONSIDERED V. Novem 4/5/04 EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conforman

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Form PTO-1449 Docket Number (Optional) **Application Number** 3351.8US (96-0223.07/US) N tyetassign d INFORMATION DISCLOSURE CITATION IN AN APPLICATION Applicant Br nt K th (Use several sheets if necessary) Filing Date July 14, 2003 Group Art Unit Unkn **U.S. PATENT DOCUMENTS EXAMINER** DOCUMENT NUMBER DATE FILING DATE INITIAL NAME CLASS SUBCLASS IF APPROPRIATE 5.940.321 08/1999 Takeuchi et al. 5,949,698 09/1999 Shirley 6,005,265 12/1999 Kuroda et al. 6,018,172 01/2000 Hidaka et al. 6,034,879 03/2000 Min et al. 6.043.562 03/2000 Keeth 6,084,307 07/2000 Keeth 6,094,370 07/2000 Takashima 6,185,123 02/2001 Allen et al. 6,188,598 02/2001 Mueller et al. 6,222,275 04/2001 Keeth 6,243,311 06/2001 Keeth **FOREIGN PATENT DOCUMENTS** Translation DOCLIMENT NUMBER DATE COUNTRY CLASS SUBCLASS YES NO VisiQ. Nessian PHINERY EXEMINE OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.) IBM Technical Disclosure Bulletin, Vol. 30, No. 3, August 1987, pps. 1314-1315. IBM Technical Disclosure Bulletin, Vol. 30, No. 11, April 1988, pps. 246-248. DATE CONSIDERED **EXAMINER** Primary Examiner V. Noncejon EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conforman not considered. Include copy of this form with next communication to the applicant.

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